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Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor: **SHIH-SHIUNG CHEU, YEA-DEAN SHEU AND CHIH-HENG SHEN**

For: **A COST EFFECTIVE POLYMIDE PROCESS TO SOLVE PASSIVATION EXTRUSION OR DAMAGE AND SOG DELAMINATES**

Enclosed are:

[X] **6** sheets of drawing(s) - formal.

[X] An assignment of the invention to **Taiwan Semiconductor Manufacturing Company**

[ ] An associate power of attorney

The filing fee has been calculated as shown below:

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TOTAL CLAIMS	**30** -20=	**10**	x 18 =	**$ 180.**
INDEP CLAIMS	**2** -3=	**0**	x 78 =	**$ 0.**
MULTIPLE DEPENDENT CLAIM PRESENTED			+ 260 =	
			SUB TOTAL	**$ 940.**
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Respectfully submitted,

STEPHEN B. ACKERMAN, REG. NO. 37,761

TS98-403

A COST EFFECTIVE POLYIMIDE PROCESS TO SOLVE PASSIVATION EXTRUSION OR DAMAGE AND SOG DELAMINATES

BACKGROUND OF THE INVENTION

(1) Field of the Invention.

The invention relates to the fabrication of Semiconductor integrated circuit devices, and more particularly to a cost effective method for forming a passivation layer on the top surface of interconnecting metal lines such that damage and extrusion in the surface of the passivation layer and SOG delamination over the metal lines are eliminated.

(2) Description of Prior Art.

Metal lines of the various layers of conducting lines in a semiconductor device are separated by insulating layers such as silicon oxide and oxygen-containing polymers that are deposited using Chemical Vapor Deposition (CVD) techniques. The insulating layers are deposited over patterned layers of interconnecting lines where electrical contact between successive layers of interconnecting lines is established with metal vias created for this purpose in the insulating layers. Electrical contact to the chip is typically established by means of bonding pads that form

electrical interfaces with patterned levels of interconnecting metal lines. Signal lines and power/ground lines can be connected to the bonding pads. After the bonding pads have been created on the surfaces of the chip package, the bonding pads are passivated and electrically insulated by the deposition of a passivation layer over the surface of the bonding pads. Passivation layer can contain silicon oxide/silicon nitride (SiO_2/Si_3N_4) deposited by CVD. The passivation layer is patterned and etched to create openings in the passivation layer for the bonding pads after which a second and relatively thick passivation layer is deposited that further insulates and protects the surface of the chips from moisture and other contaminants and from mechanical damage during the final assembling of the chips. The chips are diced and further assembled on a single or multiple chip carrier, electrical contacts are then further established to the chips via the chip bonding pads.

The trend in the semiconductor industry to create ever denser circuit packages has resulted in packaging many integrated circuit chips in one package and to provide electrical interconnects between the chips within the package. One frequently used method where multiple chips are mounted in one package is the creation of a multi chip module (MCM). This

approach has led to the creation of a multilayer structure in the MCM where active chips form the module and the chips are interconnected with a pattern of conducting lines. The conducting lines typically contain doped polysilicon, refractory metal silicides and metal. Via holes are provided that interconnect different layers of conducting lines. Typical dimensions for the conducing lines are a width of 6 to 20 um and a height of 5 to 10 um, conducting lines tend to be narrow in width and thick in the vertical direction. Signal lines are created in such a way as to reduce electrical cross talk between adjacent lines which requires that the conducting lines intersect under a 90-degree angle. To achieve proper creation of the layers of conducting lines and to minimize electrical interference between lines of different layers while at the same time meeting requirements of inter-layer insulation and device reliability, the different layers of conducting line patterns must be created in planes that are essentially flat and have good planarity.

Various materials have found application in the creation of passivation layers. Passivation layer can contain silicon oxide/silicon nitride (SiO_2/Si_3N_4) deposited by CVD, passivation layer can be a photosensitive polyimide or can comprise titanium nitride. Another material often used for passivation layer is

phosphorous doped silicon dioxide that is typically deposited over a final layer of aluminum interconnect using a Low Temperature CVD process. In recent years, photosensitive polyimide has frequently been used for the creation of passivation layers. Conventional polyimides have a number of attractive characteristics for their application in a semiconductor device structure such as the ability to fill openings of high aspect ratio, a relatively low dielectric constant (about 3.2), a simple process required for the depositing of a layer of polyimide, the reduction of sharp features or steps in the underlying layer, high temperature tolerance of cured polyimide. Photosensitive polyimides have these same characteristics but can, in addition, be patterned like a photoresist mask and can, after patterning and etching, remain on the surface on which it has been deposited to serve as a passivation layer. Typically and to improve surface adhesion and tension reduction, a precursor layer is first deposited by, for example, conventional photoresist spin coating. The precursor is, after a low temperature pre-bake, exposed using, for example, a step and repeat projection aligner and Ultra Violet (UV) light as a light source. The portions of the precursor that have been exposed in this manner are cross linked thereby leaving unexposed regions (that are not cross linked) over the bonding pads. During subsequent development, the

unexposed polyimide precursor layer (over the bonding pads) is dissolved thereby providing openings over the bonding pads. A final step of thermal curing leaves a permanent high quality passivation layer of polyimide over the substrate.

For 0.5 um. and sub-half micron technologies, the spacing of the top metal becomes small enough to cause the creation of microscopic openings (keyholes) within the surface of deposited layers of passivation layers of Plasma Enhanced Oxide (PEOXIDE) or Plasma Enhanced Silicon Nitride ($PESi_3Ni_4$). The subsequently deposited photo resist that defines a passivation pattern will flow into these keyholes resulting in decreased thickness of the photo resist layer in the areas of the keyholes. This may result in damage to the passivation film during etching of the photoresist. The removal of the photoresist is a wet and dry strip process; Act 690 and NMP are used during this process and will also accumulate in the keyhole. The final step of alloying the remaining passivation layer requires elevated temperatures. The (in the keyhole) accumulated photoresist combined with the remnants of Act 690 and NMP (in the keyhole) evaporate at these elevated temperatures causing a violent chemical reaction and the extrusion of the photoresist from the keyhole.

Figs. 1 through 7 show Prior Art processes used for the deposition of passivation layers over metal layers with the creation of bond pad contact.

Fig. 1 shows a Prior Art pattern of the top layer 12 of metal for interconnecting lines and the top layer 14 of metal for the formation of a bond pad. The layers of metal are deposited on the surface of a substrate 10.

Conventional semiconductor device processing calls for the deposition of passivation layer over the entire top surface of the wafer. The passivation layer forms an insulating, protective layer that shields and protects the surface that it covers from mechanical and chemical damage during subsequent device assembly and packaging. The passivation layer must therefore have good adhesion to the underlying metal and any level of interlevel dielectric over which it is deposited, it must provide uniform step coverage so as not to hinder subsequent steps of planarization, it must be deposited in a uniform thickness, it must protest against mechanical damage such as surface scratch while it must also protect against moisture penetration, it must not introduce stress related problems while easy patterning of the passivation layer is required. It is clear that, in order to meet the requirements that are placed on the passivation layer;

the passivation layer must be thick. In many applications, the passivation layer is therefore created using two depositions of passivation material.

Fig. 2 shows the deposition of a first passivation layer 16 of Plasma Enhanced oxide. This layer 16 is a blank deposition over the pattern 12 of the top layer metal for the interconnections and over the top layer metal 14 for the bond pad. The layer 16 of PE oxide typically is about 2000 Angstrom thick. Layer 16 reduces the mechanical stress and the hydrogen content of the overall passivation layer.

Fig. 3 shows the deposition of a second passivation layer 18 of Plasma Enhanced Si_3Ni_4 over the first passivation layer 16. This second passivation layer typically is about 7000 Angstrom thick. This nitride layer protects the underlying device against environmental impact such as mechanical scratch, mobile ion impurities such as sodium atoms and against high environmental humidity. Where the spacing between the pattern of interconnect lines 12 is very small, that is 0.5 um or sub-half micron, the spacing is narrow enough that keyholes 20 will be formed on the top surface of the deposited passivation layer 18. As keyholes are defined any surface irregularities that appear in the surface of the passivation layer. These irregularities, when

observed in cross section, often have the profile of a keyhole and are therefore generally referred to as keyhole formations. Keyholes may, at times, not be directly apparent or visible on the surface of the passivation layer as open areas or pitting in the surface. Keyholes can also be hidden below the surface of the passivation layer and can demonstrate their existence by causing poor planarization of the surface of the passivation layer.

After the creation of the passivation layer, the passivation layer must now be patterned whereby the passivation layer stays in place over the regions of the interconnecting metal (for the reasons mentioned above) while openings are created for bonding pads. The bonding contact mask is used for this purpose.

Fig. 4 shows the next step in the definition and creation of a bonding pad. A layer 22 of photoresist is deposited over the passivation layer 18; this layer 22 of photoresist is patterned (24) for the bonding pad 14. During the deposition of the photoresist, the photoresist 22 will flow into the keyholes 20 and cause a thinning in area 27 of the photoresist where the keyhole exists.

The pattern 24 of photoresist is defined through exposure and develop. The removal of the photoresist exposes the areas of the planarization layers 16 and 18 that are above the bonding pad 16.

Fig. 5 shows after the passivation etch whereby the passivation layers 16 and 18 have been etched down to the bonding pad 14. A wet or dry etch can be used for the etching of the passivation layer. Typically, dry etch is recommended due to metal corrosion concerns. After the passivation etch has been completed, the remainder of the photoresist will be removed.

Fig. 6 shows a cross section after the photoresist has been removed. The keyhole 20 caused a thinning of the photoresist around the keyhole in area 27 (Fig. 5). The etching of the photoresist may therefore damage the underlying passivation layer in areas 26 and 28 of the passivation layer 18. The removal of the photoresist may also not remove all photoresist that is in the keyhole 20 due to the narrow opening of the keyhole 20.

The strip of photoresist layer 22 includes a wet strip and a dry strip process. The wet strip applies in sequence Act 690, NMP, a DI rinse and a spin-dry step. The following dry strip is

an O_2 plasma strip at PSC. During this photoresist strip process, Act 690 and NMP will also flow into the keyhole and may, due to the narrow opening of the keyhole, not be easy to remove from the opening. After the completion of the above wet and dry strip processing steps (to remove the photoresist layer) there remains in the keyhole a mixture of left-over photoresist (photoresist that could not be reached due to the narrow entrance to the keyhole) with the Act 690 and NMP that entered the keyhole during the photoresist strip process.

Act 690 is a lift-off resist stripper and contains dimethyl sulfoxide and monoethanol-ammine.

NMP is a solvent-type stripper and contains N-Methyl-pyrolidinone.

A final alloy step is required for the curing of the passivation layer. This step takes place at temperatures up to 410 degrees C. During this alloy step the remnant Act 690 and NMP in the keyhole evaporates causing a violent chemical reaction resulting in the residue Act 690 and NMP to explode and extrude the remaining photoresist from the keyhole.

Prior Art can also use, within the above-indicated processing sequence, the deposition of a layer of SOG. Fig. 7 further highlights this approach. A interconnecting lines top layer metal pattern 12 with a bond pad top layer metal 14 for the bond pad is created as before, a passivation layer 16 of 2000 Angstrom of PE oxide is deposited over the metal pattern and the exposed surface of the substrate. Next a 3150-Angstrom thick layer 30 of SOG 314 is spin-coated; the objective of this layer is to enhance planarization of the keyholes and thereby to solve the above-indicated effects of passivation layer damage and photoresist extrusion from the keyhole. Over the layer 30 of SOG 314 a 7000-Angstrom thick layer 32 of PE Si_3N_4 is deposited and the process continues as indicated above, Figs. 4 through 6. That is a layer 34 of photoresist is spin-coated, this layer is patterned (35) for the bonding pad 14, the layer 32 of PE Si_3N_4 is removed (33) above the bonding pad 12, the passivation layer 16 is removed (17) above the bond pad 14, the photoresist (34) is removed and a final alloy step is applied to the remainder of layer 32 of PE Si_3N_4.

The disadvantage of this approach is the additional cost of the SOG material and the required additional processing steps of SOG coating and SOG curing. Furthermore, SOG has the tendency to

delaminate during subsequent packaging under high stress, which is highly detrimental to overall device reliability.

US 4,733,289 (Tsurumaru) shows a resin-molded device using polyimide and nitride for passivation.

US 5,242,864(Fassberg et al.) shows a polyimide protection layer.

US 5,013,689(Yamamoto) shows a light sensitive polyimide layer used a passivation layer.

US 5,091,289(Cronin et al.) shows a photosensitive polyimide composition.

US 5,187,119(Cech et al.) shows a photosensitive polyimide and planarization process.

US 5,807,787(Fu et al.) discloses a polyimide Passivation.

SUMMARY OF THE INVENTION

A principle objective of the present invention is to eliminate the negative effect that passivation layer imperfections have on device reliability.

Another objective of the present invention is to adapt planarization technology to ultra-small line spacing technologies.

Another objective of the present invention is to eliminate the effect of the formation of keyholes in dielectrics deposited within ultra-small line spacing.

Another objective of the present invention is to eliminate damage of cracking and delamination in the passivation layer caused by Spin-On-Glass technology.

Another objective of the present invention is to eliminate the Spin-On-Glass processing step.

Another objective of the present invention is to allow the deposition of thick and cross-link polyimide film thus preventing etching damage to the passivation layer.

Another objective of the present invention is to allow not having to remove the polyimide film from the wafer after etching thus further reducing the negative effect of keyhole extrusions.

The present invention teaches the creation of a pattern of top level metal for interconnecting lines and bond pads. A double layer of passivation is formed over the metal patterns, the present invention teaches the deposition of a thick layer of photosensitive polyimide over the passivation layers. This thick layer of photosensitive polyimide is patterned to expose the underlying bonding pads.

Key to the present invention is that the photosensitive polyimide is, after patterning for the bonding pad, not removed from the surface of the passivation layers. This thick layer of polyimide provides excellent protection of the passivation film that remains in place above the interconnecting lines. The polyimide further reduces stress during device packaging and it

solves the problem of (the Prior Art) delamination of the SOG. The step of photoresist stripping has also been eliminated.

BRIEF DESCRIPTION OF THE DRAWING.

Fig. 1 shows a cross section of the formation of a Prior Art metal pattern for interconnecting lines and a bond pad.

Fig. 2 shows a cross section of the Prior Art deposition of the first passivation layer.

Fig. 3 shows a cross section of the Prior Art deposition of the second passivation layer with the formation of a keyhole.

Fig. 4 shows a cross section of the Prior Art deposition of a photoresist layer with the patterning of this photoresist layer for the bond pad.

Fig. 5 shows a cross section of the Prior Art etching of the passivation layers.

Fig. 6 shows a cross section after Prior Art photoresist strip.

Fig. 7 shows the cross section of Prior Art SOG planarization.

Fig. 8 shows a cross section of the deposition of passivation layers, the deposition of a layer of polyimide and the patterning of the bond pad of the invention.

Fig. 9 shows a cross section of the final wafer of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 8 shows pattern 14 which is the top layer metal for the interconnecting lines and pattern 12 which is the top layer metal for the bond pad.

A first passivation layer 16 of Plasma Enhanced oxide is deposited over the metal patterns 12 and 14. This first passivation layer 16 is a blank deposition over pattern 12 and over the pattern 14 for the bond pad. The first passivation layer 16 of PE oxide is typically about 2000 Angstrom thick.

The first passivation layer is deposited using PECVD technology at a temperature between about 350 and 450 degrees C.

with a pressure of between about 2.0 and 2.8 Torr for the duration between about 8 and 12 seconds.

Fig. 8 further shows the deposition of a second passivation layer 18 of Plasma Enhanced Si_3Ni_4 over the first passivation layer 16. This second passivation layer 18 is typically about 7000 Angstrom thick. Keyhole 20 is again formed between the interconnect line pattern 12.

The second passivation layer 18 is deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 4.0 and 5.0 Torr for the duration between about 50 and 60 seconds.

Fig. 8 further shows the deposition of a layer 36 of photosensitive polyimide. The polyimide is spun on in liquid form (a polyamic precursor). It must be noted that layer 36 is a thick layer of polyimide (typically between 5.0 and 9.5 um), the result is that the concavity of keyhole 20 does not cause any significant lack of planarity of the surface of layer 36 above the keyhole 20.

This step of coating of the polyimide is performed at room temperature and ambient pressure for a time of between about 30

and 40 seconds. The indicated processing parameters are not critical since the polyimide thickness is controlled by spin speed.

The layer 36 of polyimide serves as the masking layer for patterning the bond pad 14 and replaces the Prior Art layer of photoresist to define the bond pad 14. The surface of layer 36 of polyimide is exposed to UV light to define bond pad 14, the polyimide 38 that is not exposed to the UV light is removed during developing of the polyimide. The unexposed polyimide is removed during developing with a solvent no polyimide etching is required.

The remaining (after develop) polyimide is cured to cross-link in order to protect the device circuitry. This step is a high temperature cure, typically at 350 degrees C. for 120 minutes.

Next the 2000 Angstrom layer 42 (the first passivation layer that is above the bond pad) of PE oxide and the 7000 Angstrom layer 40 (the second passivation layer that is above the bond pad) of PE SiN_3 are etched above the bond pad 14 to expose the surface of the bonding pad 14. The polyimide that is

not above the bond pad remains on the wafer and serves as a stress buffer during further device packaging.

Layers 40 and 42 are etched using the same dry etcher.

Layer 42 of the first passivation layer PE oxide is etched (above and aligned with the bond pad) using Ar/CF_4 as an etchant at a temperature of between about 120 and 160 degrees C. and a pressure of between about 0.30 and 0.40 Torr for a time of between about 33 and 39 seconds using a dry etch process.

Layer 40 of the second passivation layer of PE SiN_3 is etched (above and aligned with the bond pad) using He/NF_3 as an etchant at a temperature of between about 80 and 100 degrees C. and a pressure of between about 1.20 and 1.30 Torr for a time of between about 20 and 30 seconds using a dry etch process.

The invention offers the added advantage that the remaining passivation film is well protected by the layer of cross-linked thick polyimide and will therefore not be damaged by plasma etching. In addition, no stripping of photoresist is required since the invention leaves the thick layer of polyimide in place to serve as a stress buffer during packaging operations.

Therefore, no extrusion takes place during the formation of the bond pad.

Fig. 9 shows a cross section of the final wafer configuration. Shown are top level metal 12 for the interconnecting lines, top level metal 14 for the now exposed bond pad, the remainder 44 of the first passivation layer, the remainder 46 of the second passivation layer and the remainder 48 of the thick layer of polyimide. Layer 48 of polyimide is, at the end of the indicated process, submitted to a curing cycle.

The curing of polyimide layer 48 takes place at a temperature of 350 degrees C. in a N_2 gas environment for a time of 20 hours and a pressure of 760 Torr.

It must be noted that the use of polyimide films as inter-level dielectrics has been pursued as a technique for providing partial planarization of a dielectric surface. Polyimides offer numerous advantages for such applications such as the filling of small openings without producing voids, the ability to withstand high temperatures without dielectric breakdown, simple processing requirements, they produce surfaces in which the step heights of underlying features are reduced, step slopes which are gentle and smooth and an acceptable dielectric constant.

The created layer 48 of polyimide serves as stress buffer during the packaging process while it also solves the problems of delamination that have been observed when using the SOG planarization process (Fig. 7).

In summation: by replacing the use of photoresist with photosensitive polyimide to define the bond pad, the invention solves:

- the problem of surface damage to the passivation layer of interconnecting metal line
- the problem of providing a surface stress buffer while not having to remove photoresist
- the problem of SOG planarization
- the problem of SOG surface cracking and delamination
- the problems of an additional polyimide process to reduce stress impact on the surface of the passivation layer of the bonding pad
- the problems of keyhole formation on the surface of the planarization layer of the bonding pad

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will

recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.

What is claimed is:

1. A method for forming bonding pads of a semiconductor substrate comprising the steps of:

Providing top layer metal for interconnecting lines and top level metal for bond pads said top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the top level metal being separated by intra-layer dielectric;

Depositing a passivation layer over said top-level metal and over the exposed surface of said intra-level dielectric;

Depositing a layer of photosensitive polyimide over said passivation layer;

Patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads;

Patterning and etching said passivation layer thereby exposing said bond pad;

Curing and cross-linking said photosensitive polyimide.

2. The method of claim 1 wherein said top level metal contains Aluminum.

3. The method of claim 1 wherein said top level metal contains aluminum/copper (Al/Cu) alloy.

4. The method of claim 1 wherein the thickness of said bond pad is the thickness of said top level metal said thickness being within the range of between 4000 and 8000 Angstroms.

5. The method of claim 1 wherein said passivation layer is a first passivation layer of Plasma Enhanced oxide deposited to a thickness of about 2000 Angstrom over which a second passivation layer of Plasma Enhanced Si_3N_4 is deposited to a thickness of about 7000 Angstrom.

6. The method of claim 5 wherein said first passivation layer is deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 2.0 and 2.8 Torr for the duration between about 8 and 12 seconds.

7. The method of claim 5 wherein said second passivation layer is deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 4.0 and 5.0 Torr for the duration between about 50 and 60 seconds.

8. The method of claim 1 wherein the thickness of said photosensitive polyimide is within the range of between 5.0 and 9.5 um Angstrom after deposition of said photosensitive

polyimide whereby shrinkage of up to 40% of said thickness could occur after curing of said layer of photosensitive polyimide.

9. The method of claim 1 wherein said patterning said layer of photosensitive polyimide is creating a pattern that is above and mates with said plurality of bond pads.

10. The method of claim 1 wherein said etching said layer of photosensitive polyimide is etching through said photosensitive polyimide down to the surface of said passivation layer thereby removing said photosensitive polyimide above said bond pads.

11. The method of claim 1 wherein said patterning and etching of said photosensitive polyimide is achieved cross-linking with ultra-violet radiation through a mask while masking from UV exposure polyimide regions that are above and mate with said bond pads and further dissolving away in a solvent the non-cross-linked polyimide over the bond pads.

12. The method of claim 1 wherein that portion of said photosensitive polyimide that remains after completion of said patterning and etching said photosensitive polyimide is not removed but is left in place to serve as a stress buffer and to

thereby provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching.

13. The method of claim 1 wherein said patterning and etching said passivation layer is removing said first and said second passivation layer above and to the top metal of said bond pads.

14. The method of claim 13 wherein said etching said first passivation layer uses Ar/CF_4 as an etchant at a temperature of between about 120 and 160 degrees C. and a pressure of between about 0.30 and 0.40 Torr for a time of between about 33 and 39 seconds using a dry etch process.

15. The method of claim 13 wherein said etching said second passivation layer uses He/NF_3 as an etchant at a temperature of between about 80 and 100 degrees C. and a pressure of between about 1.20 and 1.30 Torr for a time of between about 20 and 30 seconds using a dry etch process.

16. The method of claim 1 wherein a base layer of SiO_2 is created on the top surface of said substrate said base layer to be created prior to the creation of said top level metal layers

thereby cushioning the transition of stress between the silicon substrate and said top level metal layers.

17. The method of claim 1 wherein said top level interconnecting metal and top-level bond pad metal are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate.

18. The method of claim 1 wherein said top level interconnecting metal and top-level bond metal are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed.

19. The method of claim 1 wherein said curing and cross-linking said photosensitive polyimide is in a N_2 gas ambient at a temperature of between about 300 and 400 degrees C. for a time period between about 1.5 and 2.5 hours.

20. A method of forming planarized bonding pads within the structure of a semiconductor device comprising the steps of: providing a semiconductor substrate said semiconductor substrate to contain electrical circuits or other electrical functional components;

providing a wiring layer having wiring and having a plurality of bond pads, the wiring of said wiring layer being directly connected to said bond pads in addition to being connected to said electrical circuits or other electrical functional components within said semiconductor substrate, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, said wiring and said bond pads being separated by intra-layer dielectric;

depositing a layer of top metal over said bonding pads thereby depositing the bonding pad metal;

depositing a passivation layer over said top level metal interconnecting lines and over said top level metal bond pads and over the exposed surface of the intra-level dielectric thereby shielding said bonding pads from damage during subsequent packaging operations;

depositing a layer of photosensitive polyimide over said passivation to a thickness within the range of between 5.0 and 9.5 um Angstrom;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern of photosensitive polyimide said pattern being identical to the pattern of said bond pads;

etching said layer of photosensitive polyimide thereby removing said photosensitive polyimide above said planarized bond pads; and

curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry.

21. The method of claim 20 wherein said top level metal contains aluminum.

22. The method of claim 20 wherein said top level metal contains aluminum/copper (Al/Cu) alloy.

23. The method of claim 20 wherein the thickness of said bonding pad is the thickness of said top level metal said thickness being within the range of between 4000 and 8000 Angstroms.

24. The method of claim 20 wherein said passivation layer is a first passivation layer of Plasma Enhanced oxide deposited to a thickness of about 2000 Angstrom over which a second passivation layer of Plasma Enhanced Si_3N_4 is deposited to a thickness of about 7000 Angstrom.

25. The method of claim 20 wherein said patterning said layer of photosensitive polyimide is creating a pattern that is above and mates with said plurality of bond pads.

26. The method of claim 20 wherein said etching said layer of photosensitive polyimide is etching through said photosensitive polyimide down to the surface of said bond pads.

27. The method of claim 20 wherein that portion of said photosensitive polyimide that remains after completion of said patterning and etching said photosensitive polyimide is not removed but is left in place to serve as a stress buffer and to thereby provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching.

28. The method of claim 20 wherein said patterning and etching said passivation layer is removing said passivation layer above and to the top metal of said bond pads.

29. The method of claim 20 wherein a base layer of SiO_2 is created on the top surface of said substrate said base layer to be created prior to the creation of said top level metal thereby

cushioning the transition of stress between the silicon substrate and said wiring layer.

30. The method of claim 20 wherein said curing and cross-linking said photosensitive polyimide is in a N_2 gas ambient at a temperature of between about 300 and 400 degrees C. for a time period between about 1.5 and 2.5 hours.

ABSTRACT

The present invention teaches the deposition of a pattern of interconnecting lines and bond pads. Passivation layers are deposited over this metal pattern. A layer of photosensitive polyimide is deposited over the passivation layers. This layer of photosensitive polyimide is patterned, exposed and developed to expose the underlying bonding pads. The remaining polyimide is cured and cross-linked and remains in place to serve as a buffer during further device packaging. Key to the present invention is that the remaining photosensitive polyimide is not removed after the bond pad has been exposed.

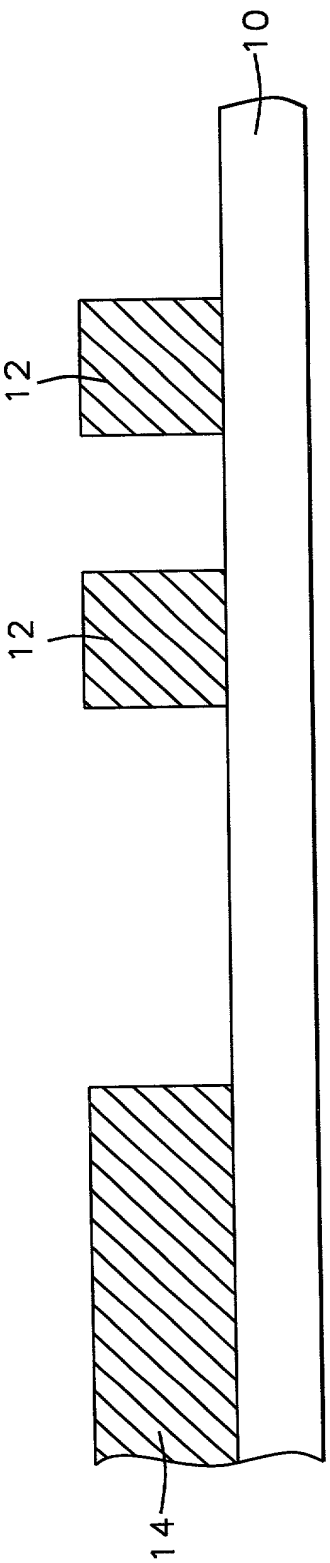

FIG. 1 - Prior Art

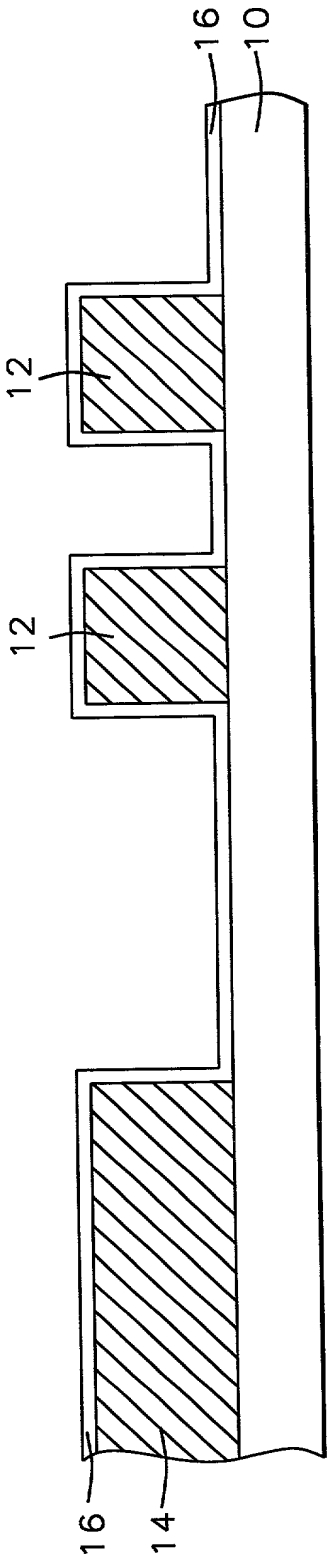

FIG. 2 - Prior Art

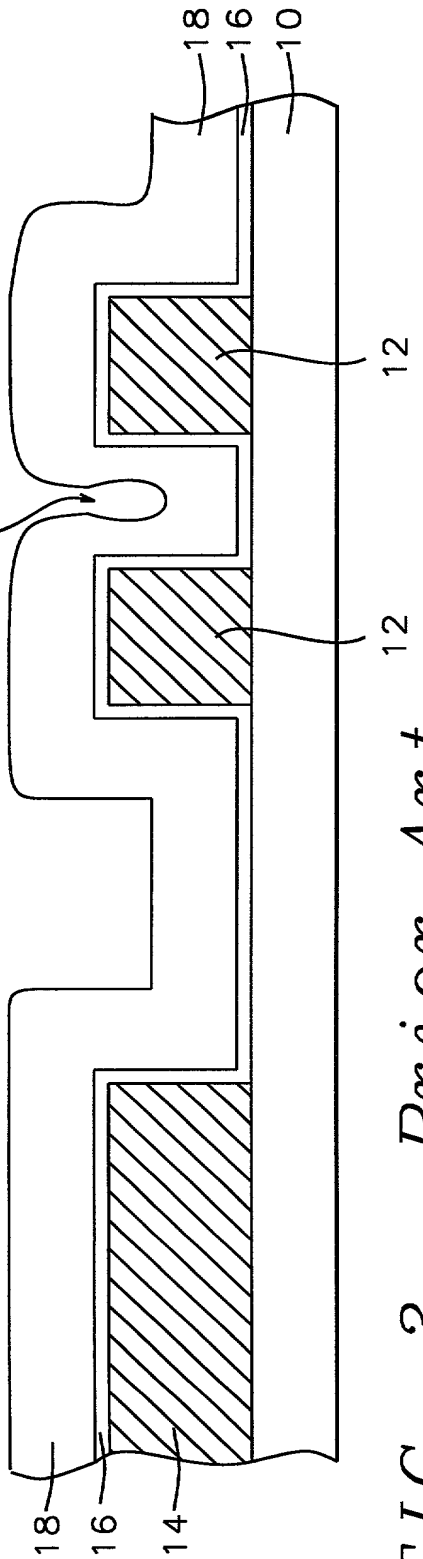

FIG. 3 - Prior Art

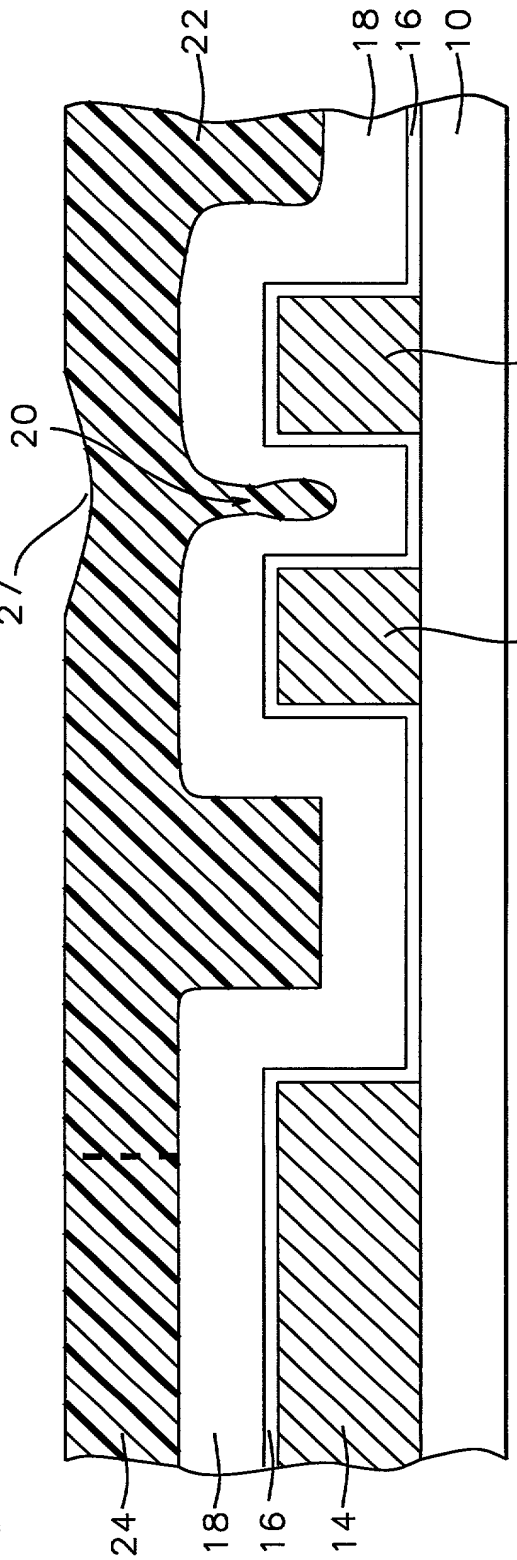

FIG. 4 - Prior Art

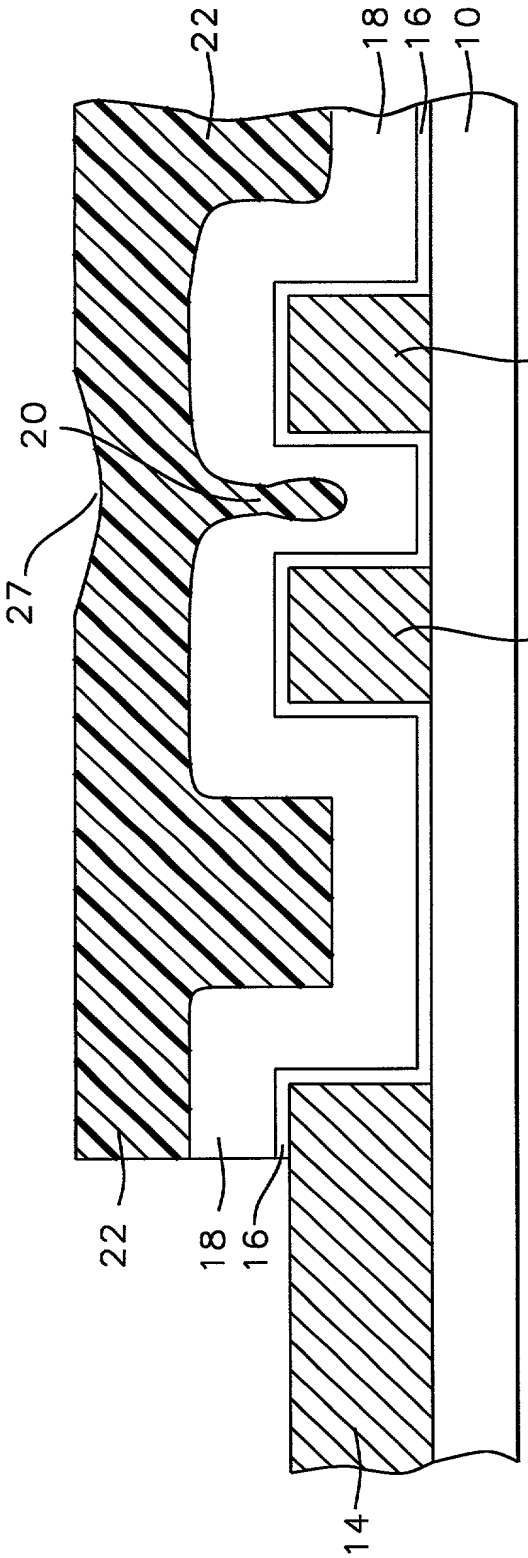

FIG. 5 – Prior Art

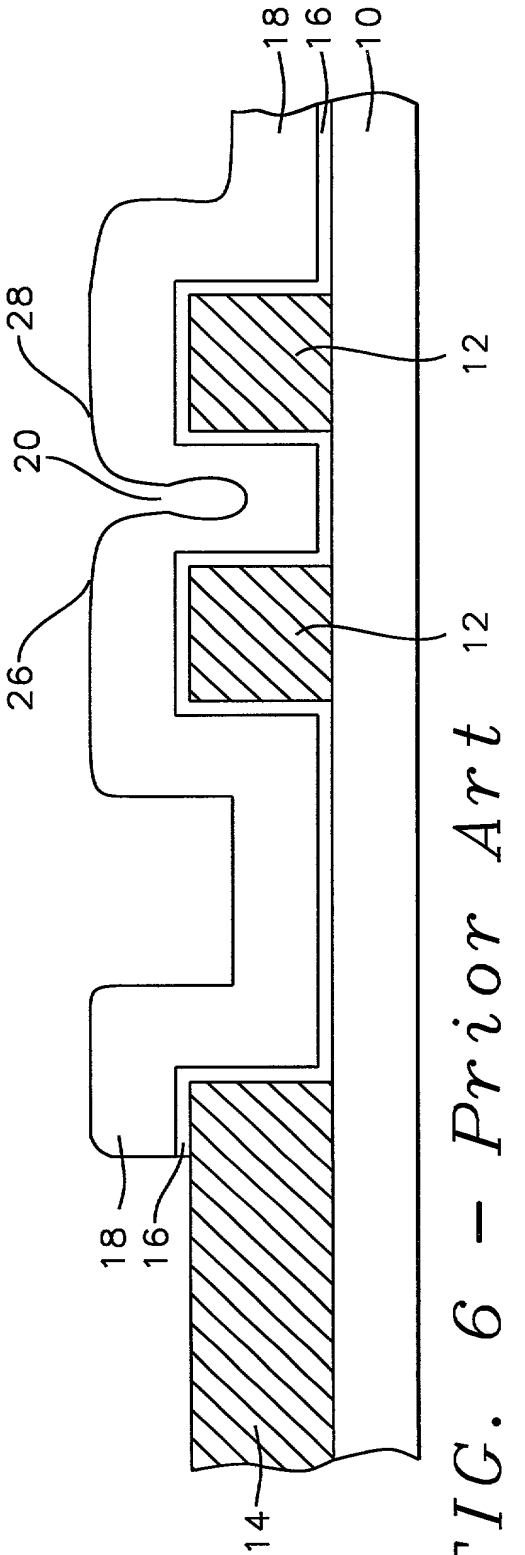

FIG. 6 – Prior Art

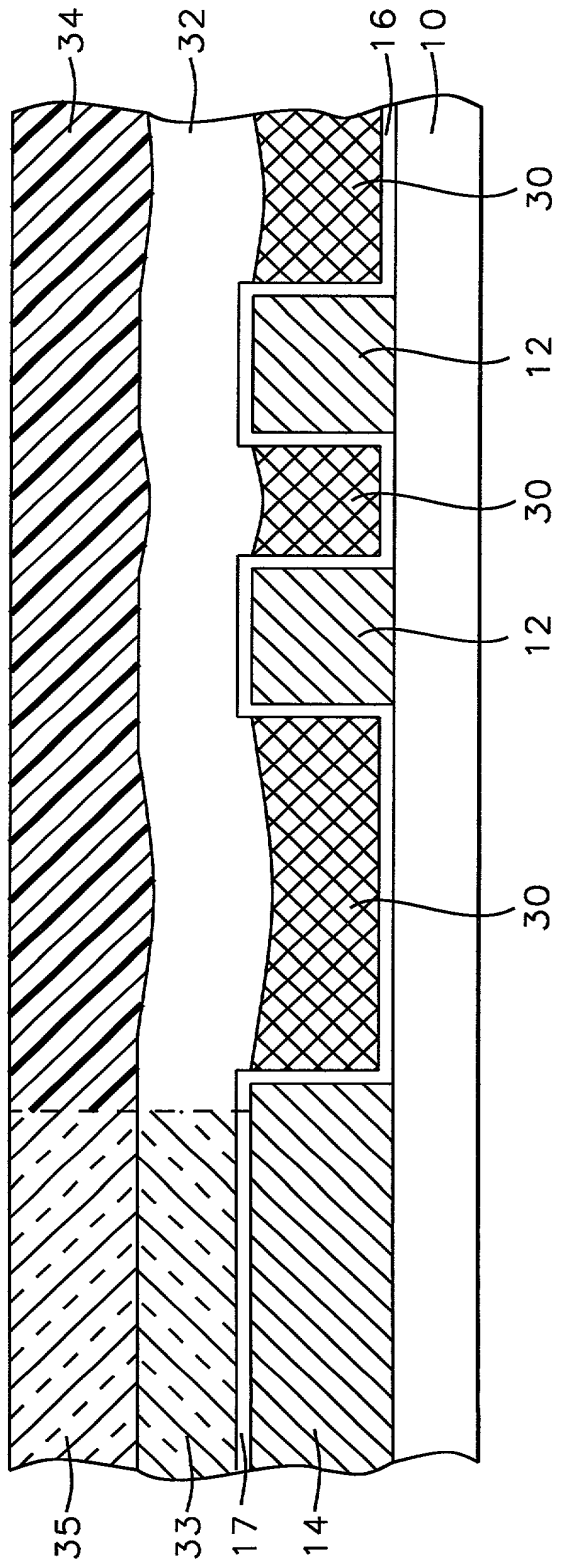

FIG. 7 - Prior Art

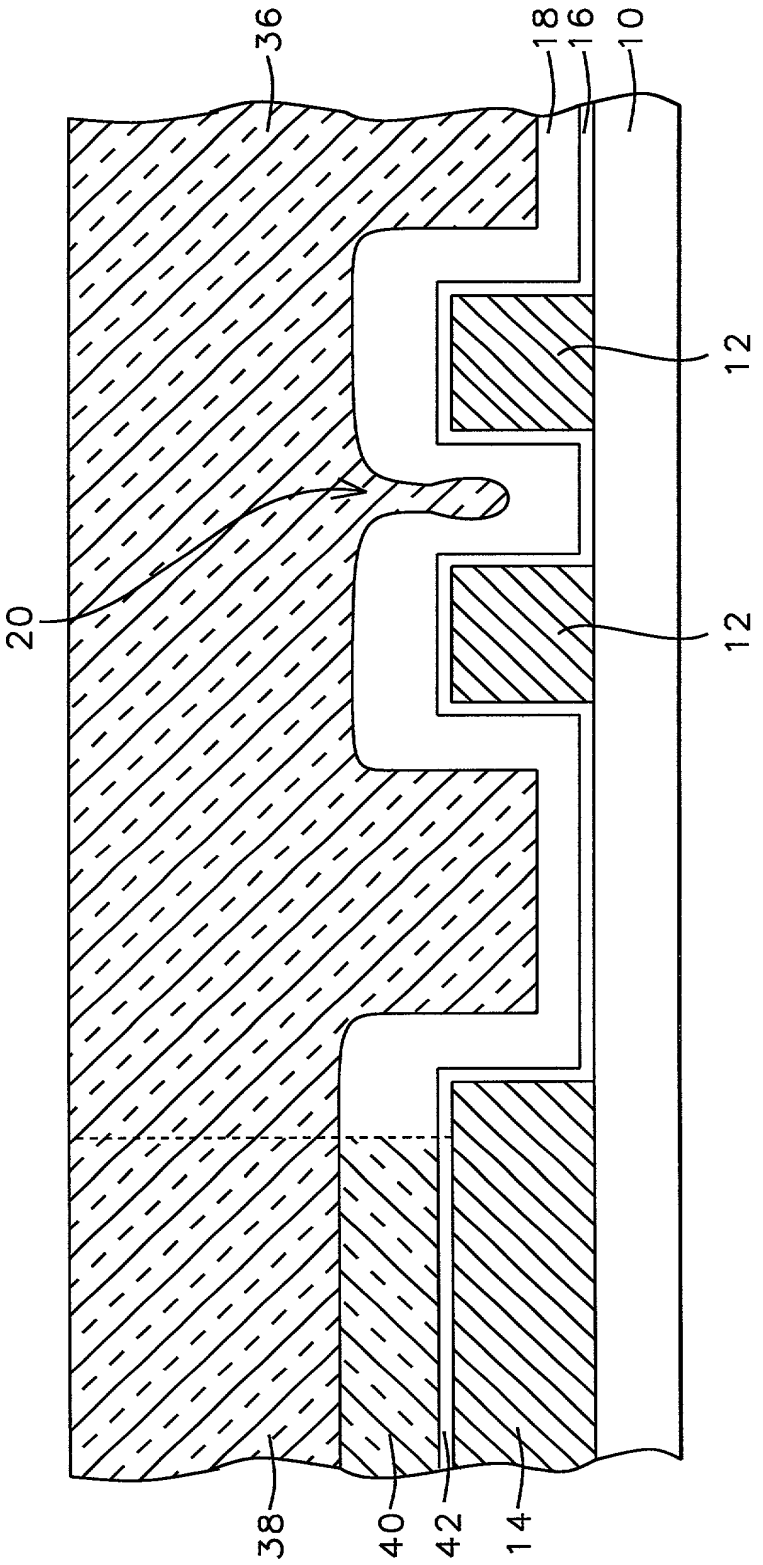

FIG. 8

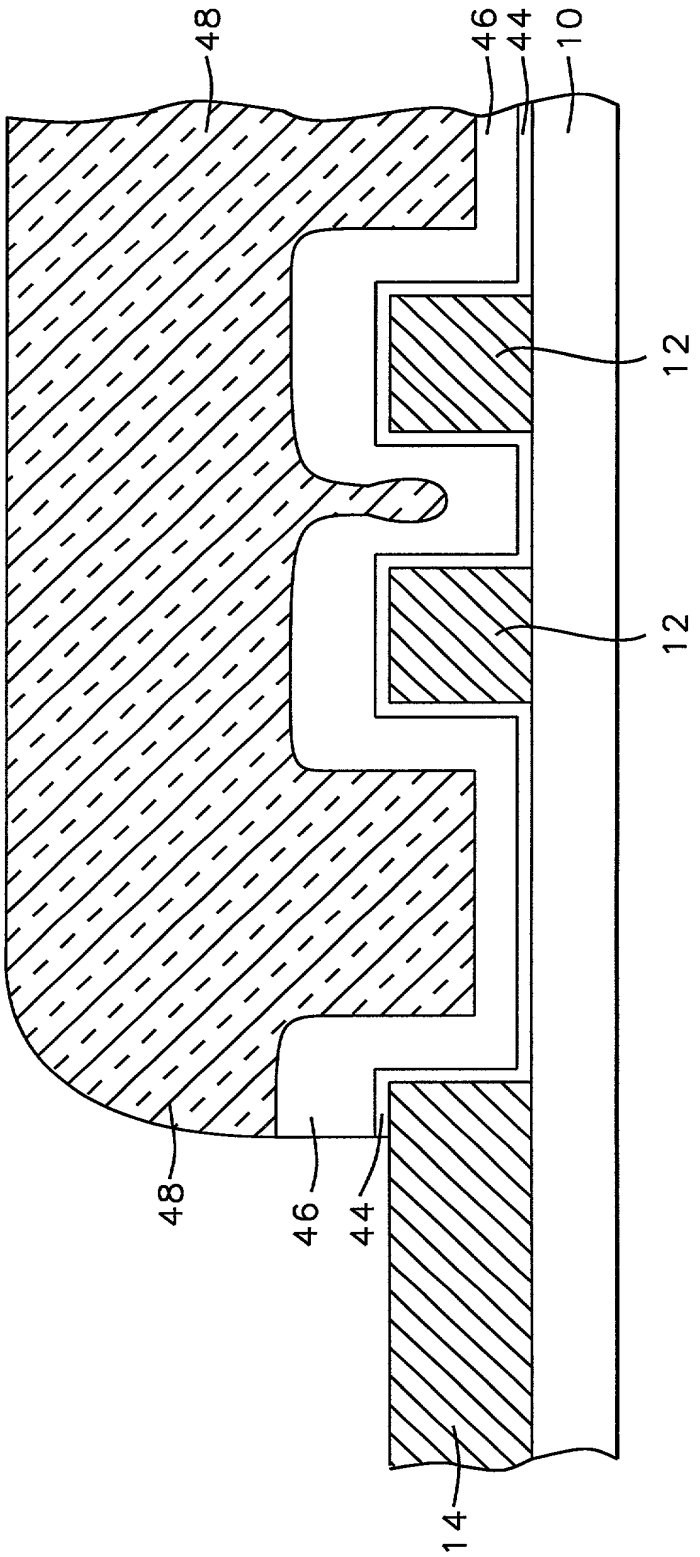

FIG. 9

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. **TS98-403**

As a below named Inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **A Cost Effective Polymide Process To Solve Passivation Extrusion Or Damage And SOG Delaminates**

the specification of which (check one)

X is attached hereto.

was filed on _____

Application Serial No. _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above Identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed:

(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name & registration no.)

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Full name of **sole or first** inventor — Date

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Date

Inventor's signature

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Citizenship

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Full name of **fifth** inventor

Date

Inventor's signature

Residence

Citizenship

Post Office Address

Full name of **sixth** inventor

Date

Inventor's signature

Residence

Citizenship

Post Office Address